REMARKS

This is intended as a full and complete response to the Final Office Action dated November 24, 2003, having a shortened statutory period for response set to expire on February 24, 2004. Claims 1-60 remain pending in the application and are shown above. Claims 1-60 are rejected. Reconsideration of the rejected claims is requested for reasons presented below.

Claims 1-24 stand rejected under 35 U.S.C. § 102(e) as being anticipated by *Shroff et al.*, U.S. Patent No. 6,515,343. The Examiner asserts that *Shroff et al.* discloses the aspects of the invention recited in claims 1-24. Applicants respectfully respond to this rejection.

Shroff et al. discloses forming an antifuse structure between two layers having damascene structures formed therein. (*See*, col. 3, lines 62, to col. 6, line 28.)

Shroff et al. does not teach, show, or suggest forming a feature definition in a dielectric material deposited on a surface of a substrate, depositing one or more conductive materials to fill at least a portion of the feature definition, planarizing the one or more conductive materials to expose the dielectric material, etching at least a portion of the dielectric material exposed by the planarizing the one or more conductive materials, and depositing a low k dielectric material to replace the dielectric material removed by the etching at least a portion of the dielectric material, as recited in claim 1, and claims dependent thereon. Withdrawal of the rejection is respectfully requested.

Claims 25-26, 28-40 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Shroff et al.*, U.S. Patent No. 6,515,343 in view of *Ning*, U.S. Patent No. 6,323,067. The Examiner asserts that it would have been obvious to one skilled in the art to substitute *Shroff et al.*'s SiN dielectric layer with an oxide layer deposited by PECVD/self-planarizing dielectric layer as taught by *Ning*. Applicant respectfully traverses the rejection.

Shroff et al. is described above. *Ning* discloses a light absorption layer deposited onto a dielectric layer having an interconnect positioned below. *Ning* does not suggest or motivate planarizing a conductive barrier layer and a conductive material to expose one or more dielectric layers, etching the one or more dielectric layers exposed by the

planarizing the conductive barrier layer and the conductive material, depositing a low k dielectric material on the substrate to replace the one or more dielectric layers removed by the etching at least a portion of the one or more dielectric layers.

Thus, the combination of *Shroff et al.* and *Ning* does not teach, show, or suggest depositing one or more dielectric layers on a substrate, etching the one or more dielectric layers to form a dual damascene definition therein, the dual damascene definition having a vertical interconnect and a horizontal interconnect, depositing a conductive barrier layer over exposed surfaces of the dual damascene definition, depositing a conductive material over the conductive barrier layer to fill at least a portion of the dual damascene definition, planarizing the conductive barrier layer and the conductive material to expose the one or more dielectric layers, etching at least a portion of the one or more dielectric layers exposed by the planarizing the conductive barrier layer and the conductive material, depositing a low k dielectric material to replace the one or more dielectric layers removed by the etching at least a portion of the one or more dielectric layers, and depositing a self-planarizing dielectric layer on the low k dielectric material, as recited in claim 25 and claims dependent thereon. Withdrawal of the rejection is respectfully requested.

Claims 27 and 43 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Shroff et al.* U.S. Patent No. 6,323,067, in view of *Ning*, U.S. Patent No. 6,323,067 and further in view of *Zhao et al.*, U.S. Patent No. 6,627,539. The Examiner asserts that it would have been obvious to one skilled in the art to modify *Shroff et al. Ning* by repeating the steps as per *Zhao et al.* Applicant respectfully traverses the rejection.

Shroff et al. and *Ning* are described above. *Zhao et al.* discloses repeating steps for forming a damascene as described as shown in Figures 2J-2L of *Zhao et al.*

The combination of *Shroff et al.*, *Ning*, and *Zhao et al.* does not teach, show, or suggest depositing one or more dielectric layers on a substrate, etching the one or more dielectric layers to form a dual damascene definition therein, the dual damascene definition having a vertical interconnect and a horizontal interconnect, depositing a conductive barrier layer over exposed surfaces of the dual damascene definition, depositing a conductive material over the conductive barrier layer to fill at least a portion of the dual damascene definition, planarizing the conductive barrier layer and the

conductive material to expose the one or more dielectric layers, etching at least a portion of the one or more dielectric layers exposed by the planarizing the conductive barrier layer and the conductive material, depositing a low k dielectric material to replace the one or more dielectric layers removed by the etching at least a portion of the one or more dielectric layers, and depositing a self-planarizing dielectric layer on the low k dielectric material, and further comprising repeating depositing a conductive barrier layer over exposed surfaces of the dual damascene definition, depositing a conductive material over the conductive barrier layer to fill at least a portion of the dual damascene definition, planarizing the conductive barrier layer and the conductive material to expose the one or more dielectric layers, etching at least a portion of the one or more dielectric layers exposed by the planarizing the conductive barrier layer and the conductive material, as recited in claim 27. Withdrawal of the rejection is respectfully requested.

The combination of *Shroff et al.*, *Ning*, and *Zhao et al.* does not teach, show, or suggest depositing a first dielectric material, depositing a second dielectric material on the first dielectric material, etching the second dielectric layer to exposed a portion of the first dielectric layer, depositing a third dielectric layer on the second dielectric material and exposed portion of the first dielectric layer, etching the first and third dielectric layers to form a vertical interconnect and a horizontal interconnect of a dual damascene definition, depositing a conductive barrier layer over exposed surfaces of the dual damascene definition, depositing a conductive material over the conductive barrier layer to fill at least a portion of the dual damascene definition, planarizing the conductive barrier layer and the conductive material to expose the one or more dielectric layers, etching the one or more dielectric layers exposed by the planarizing the conductive barrier layer and the conductive material, depositing a low k dielectric material on the substrate to replace the one or more dielectric layers removed by the etching at least a portion of the one or more dielectric layers, and depositing a self-planarizing dielectric layer on the low k dielectric material, and further comprising repeating depositing a conductive barrier layer over exposed surfaces of the dual damascene definition, depositing a conductive material over the conductive barrier layer to fill at least a portion of the dual damascene definition, planarizing the conductive

barrier layer and the conductive material to expose the one or more dielectric layers, as recited in claim 43. Withdrawal of the rejection is respectfully requested.

Claims 41-42, 44-54 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Shroff, et al.*, U.S. Patent No. 6,515,343, in view of *Ning*, U.S. Patent No. 6,323,067. The Examiner asserts that it would have been obvious to one skilled in the art to substitute *Shroff et al.*'s SiN dielectric layer with an oxide layer deposited by PECVD/self-planarizing dielectric layer as taught by *Ning*. Applicant respectfully traverses the rejection.

Shroff et al. and *Ning* are described above. *Ning* does not suggest or motivate planarizing the conductive barrier layer and the conductive material to expose the one or more dielectric layers, etching the one or more dielectric layers exposed by the planarizing the conductive barrier layer and the conductive material, depositing a low k dielectric material on the substrate to replace the one or more dielectric layers removed by the etching at least a portion of the one or more dielectric layers.

Thus, the combination of *Shroff et al.* and *Ning* does not teach, show, or suggest depositing a first dielectric material, depositing a second dielectric material on the first dielectric material, etching the second dielectric layer to exposed a portion of the first dielectric layer, depositing a third dielectric layer on the second dielectric material and exposed portion of the first dielectric layer, etching the first and third dielectric layers to form a vertical interconnect and a horizontal interconnect of a dual damascene definition, depositing a conductive barrier layer over exposed surfaces of the dual damascene definition, depositing a conductive material over the conductive barrier layer to fill at least a portion of the dual damascene definition, planarizing the conductive barrier layer and the conductive material to expose the one or more dielectric layers, etching the one or more dielectric layers exposed by the planarizing the conductive barrier layer and the conductive material, depositing a low k dielectric material on the substrate to replace the one or more dielectric layers removed by the etching at least a portion of the one or more dielectric layers, and depositing a self-planarizing dielectric layer on the low k dielectric material, as recited in claim 41 and claims dependent thereon. Withdrawal of the rejection is respectfully requested.

Claims 55-56 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Shroff, et al.* U.S. Patent No. 6,515,343, in view of *Annapragada,* U.S. Patent No. 6,303,525. The Examiner asserts that it would have been obvious to one skilled in the art to modify *Shroff et al. Ning* by using the depositing process parameters as per *Annapragada.* Applicant respectfully traverses the rejection.

Shroff et al. and *Ning* are described above. *Annapragada* discloses depositing a liner dielectric to provide improved adhesion between low dielectric constant spin-on materials among metal layers.

The combination of *Shroff et al.*, *Ning*, and *Annapragada* does not teach, show, or suggest forming a feature definition in a dielectric material deposited on a surface of a substrate, depositing one or more conductive materials to fill at least a portion of the feature definition, planarizing the one or more conductive materials to expose the dielectric material, etching at least a portion of the dielectric material exposed by the planarizing the one or more conductive materials, and depositing a low k dielectric material to replace the dielectric material removed by the etching at least a portion of the dielectric material, as recited in claim 1, and claims 55 and 56 dependent thereon. Withdrawal of the rejection is respectfully requested.

Claims 57-60 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Shroff, et al.* U.S. Patent No. 6,515,343, in view of *Ning*, U.S. Patent No. 6,323,067 and further in view of *Annapragada*, U.S. Patent No. 6,303,525. The Examiner asserts that it would have been obvious to one skilled in the art to modify *Shroff et al. Ning* by using the depositing process parameters as per *Annapragada.* Applicant respectfully traverses the rejection.

Shroff et al. Ning, and *Annapragada* are described above. The combination of *Shroff et al.*, *Ning*, and *Annapragada* does not teach, show, or suggest depositing one or more dielectric layers on a substrate, etching the one or more dielectric layers to form a dual damascene definition therein, the dual damascene definition having a vertical interconnect and a horizontal interconnect, depositing a conductive barrier layer over exposed surfaces of the dual damascene definition, depositing a conductive material over the conductive barrier layer to fill at least a portion of the dual damascene definition, planarizing the conductive barrier layer and the conductive material to expose

the one or more dielectric layers, etching at least a portion of the one or more dielectric layers exposed by the planarizing the conductive barrier layer and the conductive material, depositing a low k dielectric material to replace the one or more dielectric layers removed by the etching at least a portion of the one or more dielectric layers, and depositing a self-planarizing dielectric layer on the low k dielectric material, as recited in claim 25 and claims 57 and 58 dependent thereon. Withdrawal of the rejection is respectfully requested.

The combination of *Shroff et al.*, *Ning*, and *Annapragada* does not teach, show, or suggest depositing a first dielectric material, depositing a second dielectric material on the first dielectric material, etching the second dielectric layer to exposed a portion of the first dielectric layer, depositing a third dielectric layer on the second dielectric material and exposed portion of the first dielectric layer, etching the first and third dielectric layers to form a vertical interconnect and a horizontal interconnect of a dual damascene definition, depositing a conductive barrier layer over exposed surfaces of the dual damascene definition, depositing a conductive material over the conductive barrier layer to fill at least a portion of the dual damascene definition, planarizing the conductive barrier layer and the conductive material to expose the one or more dielectric layers, etching the one or more dielectric layers exposed by the planarizing the conductive barrier layer and the conductive material, depositing a low k dielectric material on the substrate to replace the one or more dielectric layers removed by the etching at least a portion of the one or more dielectric layers, and depositing a self-planarizing dielectric layer on the low k dielectric material, as recited in claim 41 and claims 59 and 60 dependent thereon. Withdrawal of the rejection is respectfully requested.

The secondary references made of record are noted. However, it is believed that the secondary references are no more pertinent to the Applicant's disclosure than the primary references cited in the Final Office Action. Therefore, Applicant believes that a detailed discussion of the secondary references is not necessary for a full and complete response to this Final Office Action.

In conclusion, the references cited by the Examiner, alone or in combination, do not teach, show, or suggest the invention as claimed. Having addressed all issues set out in the office action, Applicant respectfully submits that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted,

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